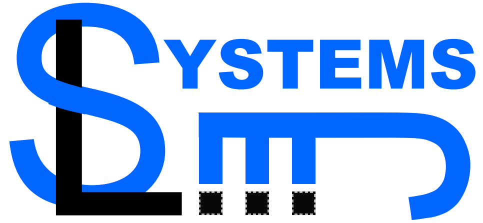
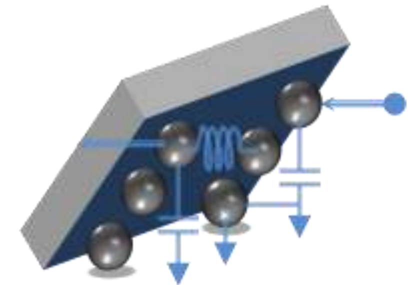
*HTTP:/WWW.SL3J.COM/ Partial printouts for our website visitors. Send your comments and requests to contact@sl 3j.com*




# Power Train Scaling for High Frequency Switching, Impact on Power Controller Design



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**IEEE PowerSoC 2010**

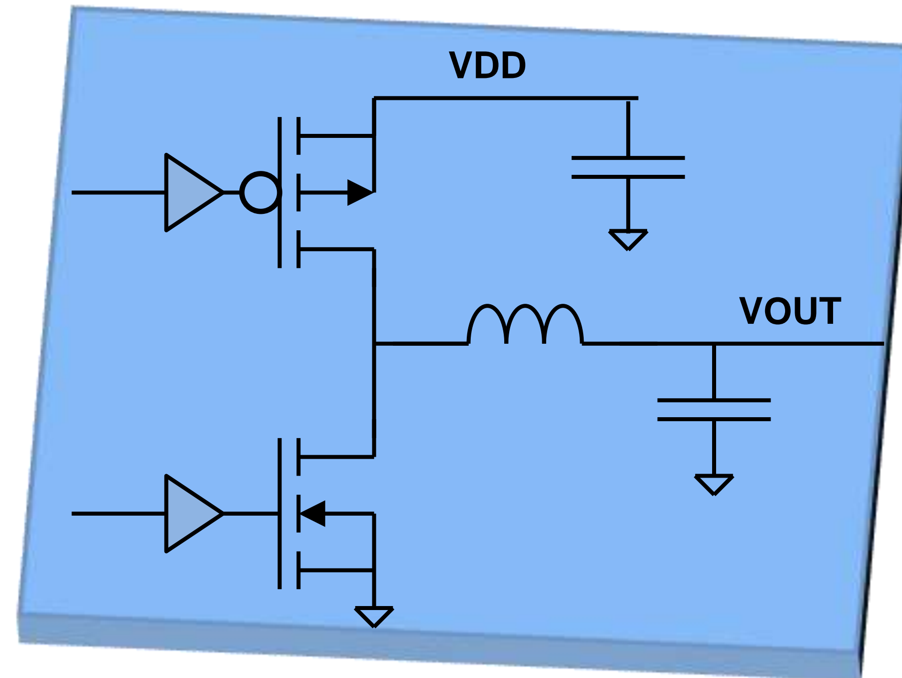
# Outline

- Background for High Frequency Switching
- Dealing with Noise
- Challenges For HF Controllers

# HF DC to DC Converters

## Challenges

- **Challenges for Technologist**
  - Ultra Fast Power Switches with High Breakdown Voltage
  - Low DCR HF Inductor
  - Low ESR Capacitor
  - **Compatible Integration Process**
    - SiP, SoC etc

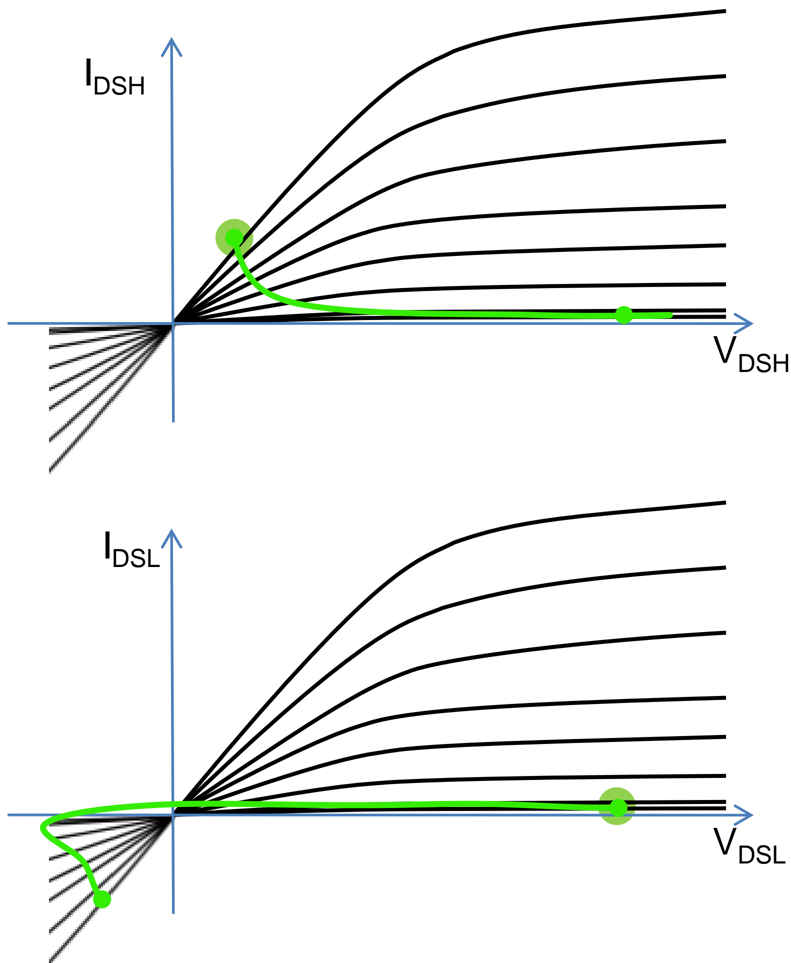


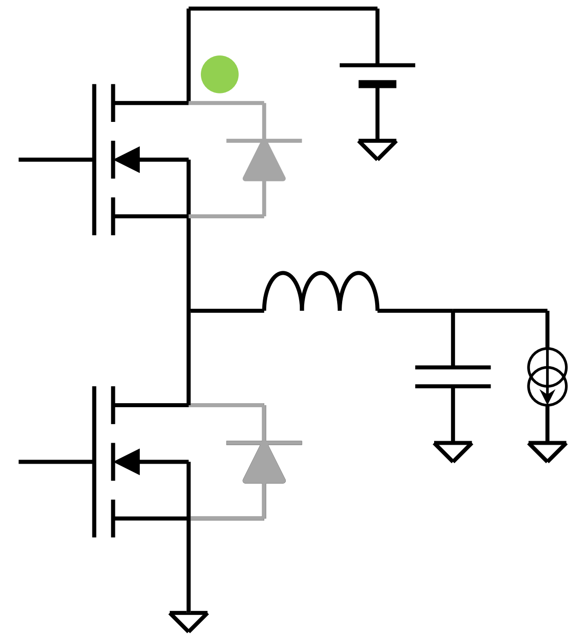

- **Challenge for Designers**
  - Voltage ringing is way higher than regulated voltage amplitude
  - Differentiate Load transients from Ringing
  - Power Consumption in PWM circuitry
  - **Construct Simple, Scalable and Exportable Design**

  - **Only Simple Ideas work efficiently**

# Background, Solid State Power Switching

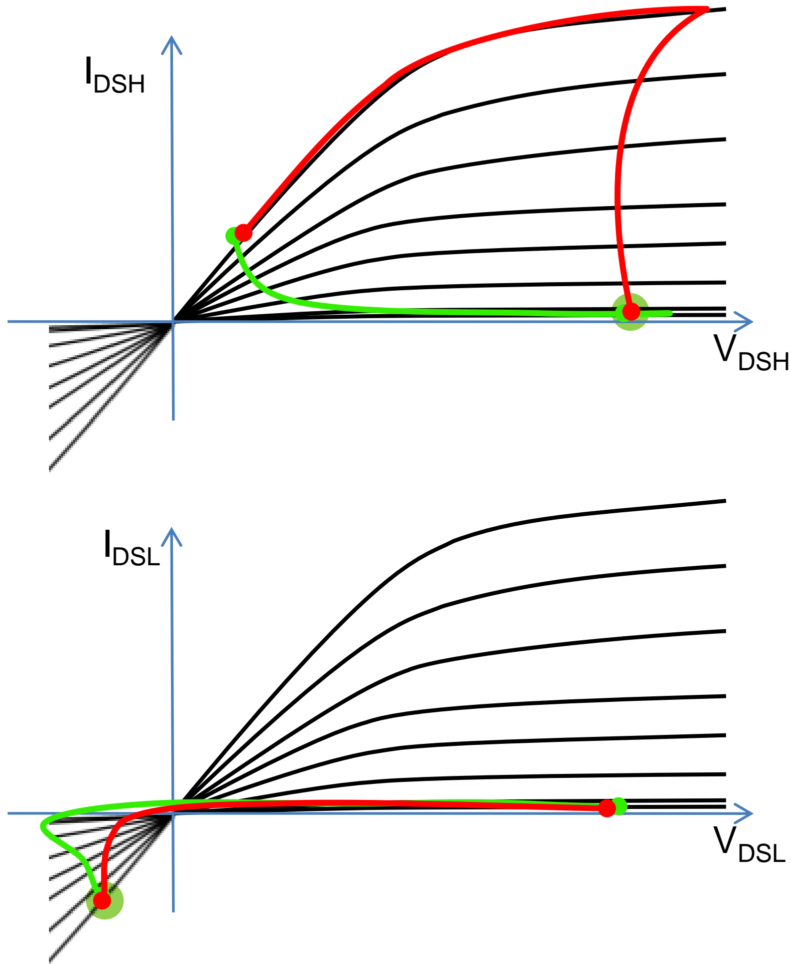
## Hi-Lo Transition

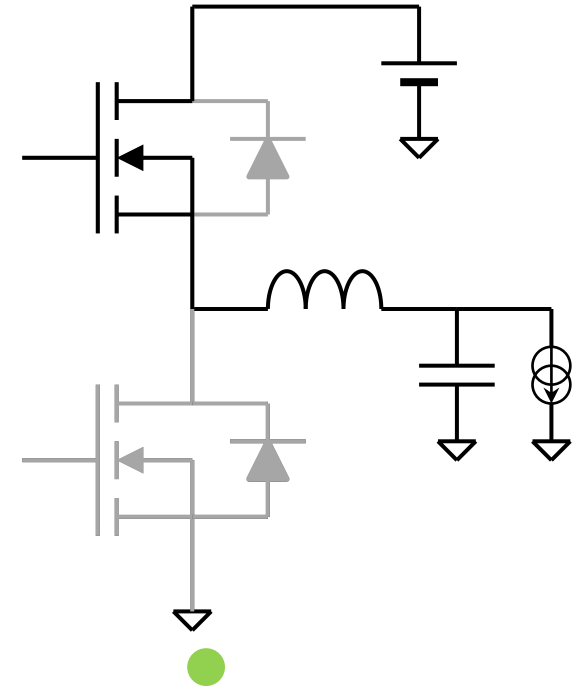


# Background, Solid State Power Switching

## Lo-Hi Transition

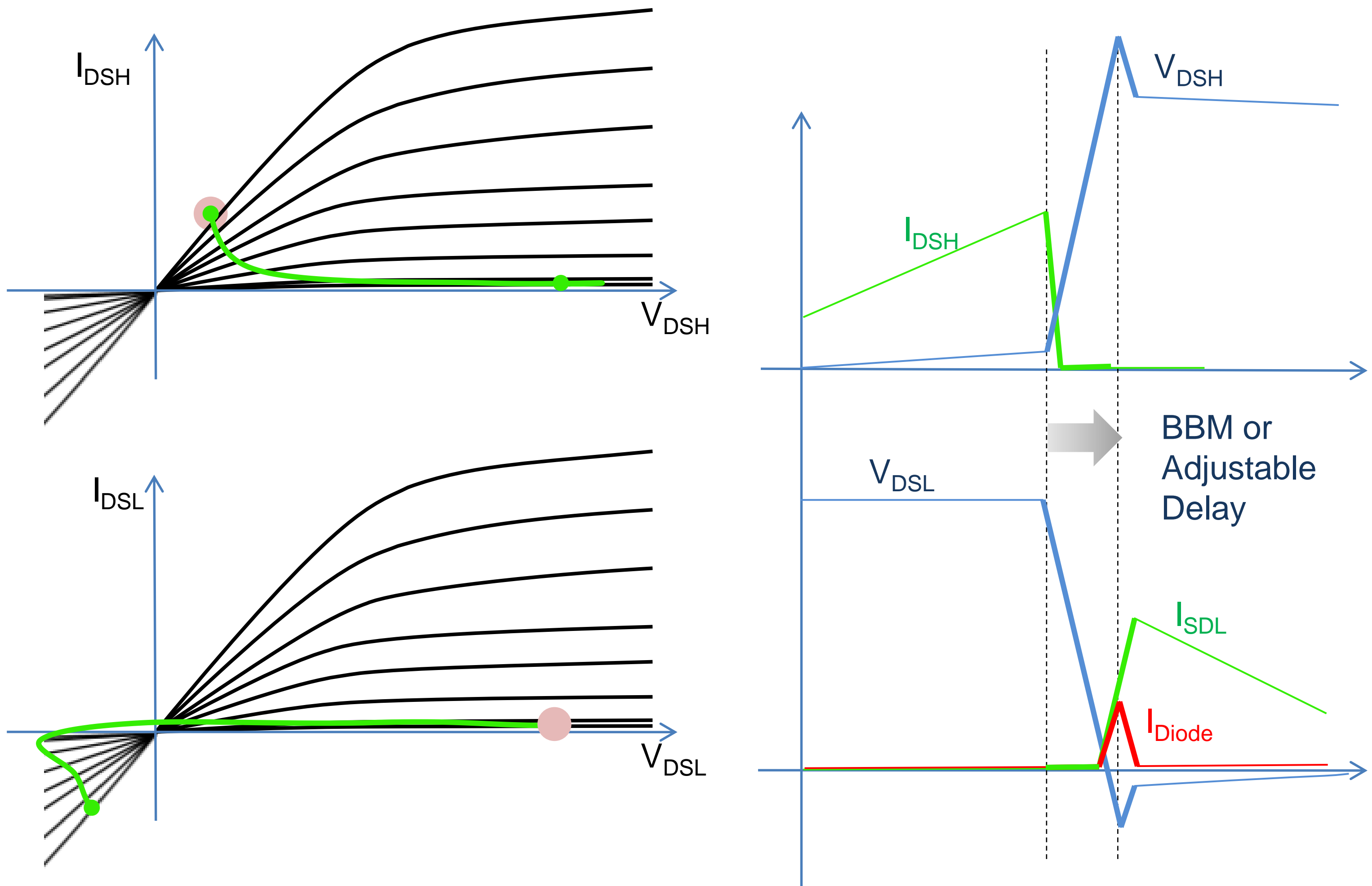


S. AJRAM, SL3J SYSTEMS SARL, Marseille France

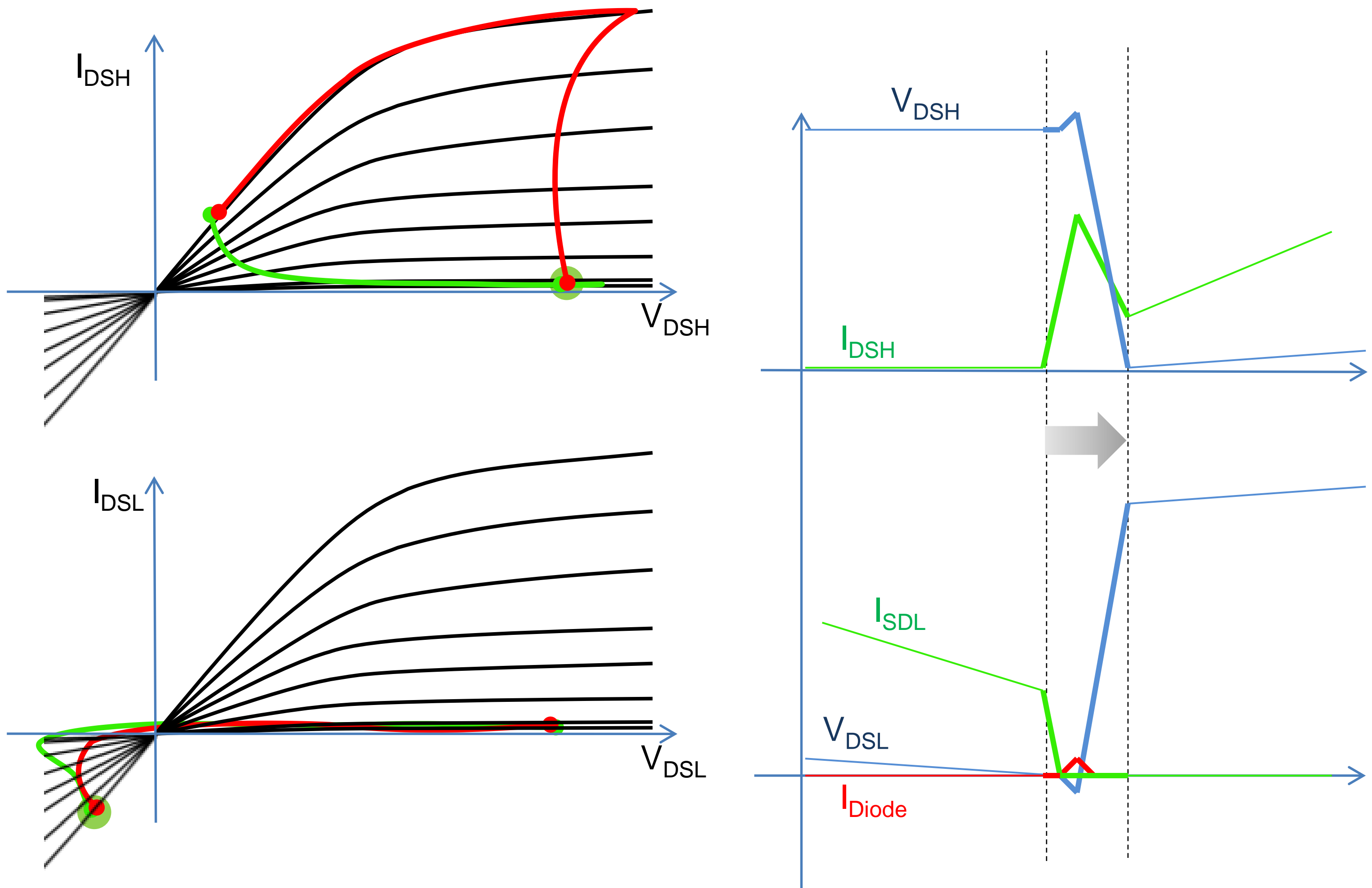
# Background, Solid State Power Switching

## Hi-Lo Transition : Waveforms



# Background, Solid State Power Switching

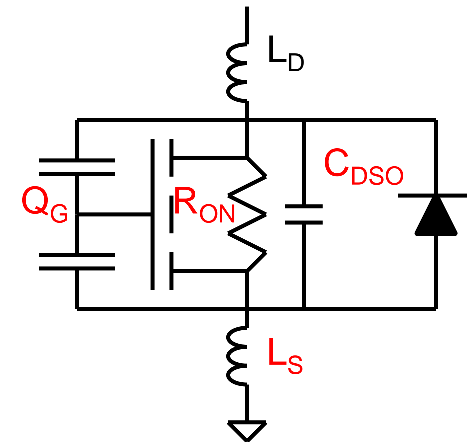
## Lo-Hi Transition : Waveforms



# Overview of Switch Power Losses
## Low Side Switch

- **Switching Losses Causes**
  - Qg Charging and discharging
  - $C_{DS}$ Charging (Discharging is often adiabatic)
  - Body diode charge recovery (losses induced at HS switch)
  - Parasitic Inductor Energy

$$P_{AC} = \frac{1}{T_0}\left(\frac{1}{2}C_{DSO}V_{DD}{}^{2} + Q_G V_{DD} + Q_R V_{DD} + \frac{1}{2}L_S I_L{}^{2}\right)$$



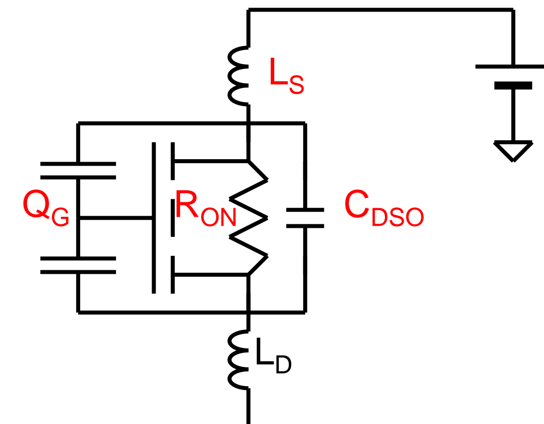

- **Conduction Losses**
  - Conduction losses in $R_{DSON}$
  - Body diode Forward losses (short time)
  - Shoot through current (use BBM)

$$P_{DC} = (1-D).R_{ON}.I_L^2 + (1-D).R_{ON}.\frac{\Delta I^2}{12} + \frac{\Delta T}{T_0}.V_F.I_L$$

# Overview of Switch Power Losses
## High Side Switch

- **Switching Losses Causes**
  - Qg Charging and discharging
  - $C_{DS}$ Discharging (Charging is often adiabatic)
  - Ids x Vds crossing at turn on
  - Parasitic Inductor Energy

$$P_{AC} = \frac{1}{T_0}\left(Q_G V_{DD} + \frac{I_L}{I_{DRV}} C_{GDO} \cdot V_{DD}{}^2 + \frac{1}{2} C_{DSO} V_{DD}{}^2 + \frac{1}{2} L_S I_L{}^2\right)$$




- **Conduction Losses**
  - Conduction losses in $R_{DSON}$
  - Shoot through current (use BBM)

$$P_{DC} = D.R_{ON}.I_L^2 + D.R_{ON}.\frac{\Delta I^2}{12}$$

# Intrinsic Limitations for Power Train Scaling

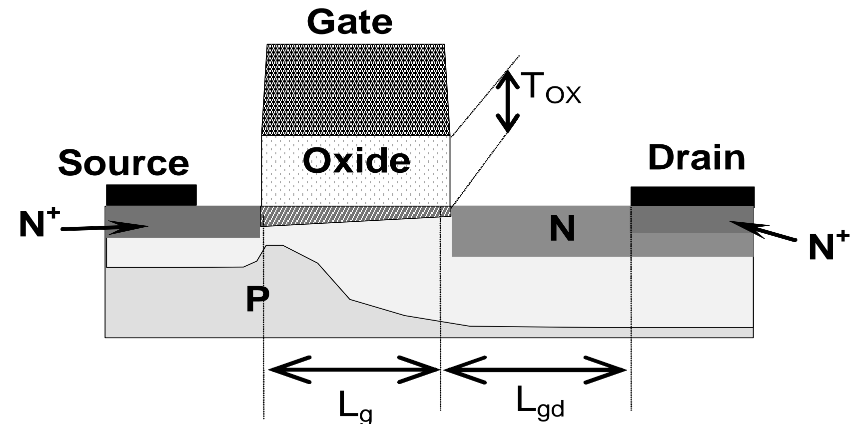
- The sum ($P_{AC}$ + $P_{DC}$) is minimum When ($P_{AC}$ = $P_{DC}$)
- Reason : $P_{AC}$ x $P_{DC}$ = Constant

$$\frac{(P_{AC}+P_{DC})_{MIN}}{P_{IN}} = \frac{2.P_{AC}}{P_{IN}} \cong \left(\frac{V_{IN}}{V_{OUT}}\right)\left(\frac{S_{PWR}}{S_{DRV}}\right) F_0 K_D$$

- ✓ Stage Scaling (20, 50, 100…)
- ✓ $K_D$ for CMOS ranges from 10ps to 100ps
- ✓ At 10MHz => for instance $F_0.K_D$ = 0.001

# Device / Process Optimization
[S. Ajram, G. Salmer, IEEE Trans. Power Electronics 2001]

| Parameter | Physics |
|---|---|
| Breakdown Voltage | $V_{dsB} \cong V_{dsubB} \cdot \left(\frac{1}{1+\beta}\right)^{\frac{1}{n}}$ |
| ($V_{BD}$) See Note (1) | $V_{dsuB} = 60.\left(\frac{E_g}{1.11}\right)^{\frac{3}{2}} \left(\frac{10^{16}}{N_A^{Channel}}\right)^{\frac{3}{4}}$ |
| On-State Resistance ($R_{ON}$) | $\frac{1}{q.N_s^D.\overline{\mu}_n^D} \frac{L_{gd}}{W_g}$ |
| Maximum Input Capacitance ($C_{in}$) | $W_g.L_g.C_{OX}$ |
| Loss Factor $k_D=C_{in}.R_{ON}$ | $\frac{L_{gd}.L_g.C_{OX}}{q.N_s^D.\overline{\mu}_n^D}$ |




Wg: Gate width
$C_{OX}$: Oxide capacitance
$V_{gsON}$: Gate-to-source on-state voltage
$V_T$: Threshold voltage
NsD, µnD: Respectively, the surface doping level and the electron mobility in the drain-to-channel lightly doped region
NA Channel: Substrate doping level under the gate
*b*: Parasitic substrate NPN transistor current gain
*vs*: Carrier saturation velocity

## Process Optimization

1. Set Breakdown Voltage 1.8V, 5V etc…
2. Breakdown determines possible Doping
3. Doping Sets Mobility
4. Engineer Lg and $T_{OX}$
5. (Mobility + Doping + Gate) Sets Loss Factor

**Note (1)** Comment by Pr. Paul Chow, RPI USA
This equation does not fit for bandgap larger than 2.5eV such as for SiC or GaN, use the following reference instead
T. Paul Chow and Ritu Tyagi "*Wide Bandgap Compound Semiconductors for Superior High-Voltage Unipolar Power Devices*" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 41, NO. 8, AUGUST 1994

# Slides to be requested