Impact of the Output Capacitor Selection on Switching DCDC Noise Performance

I. Introduction

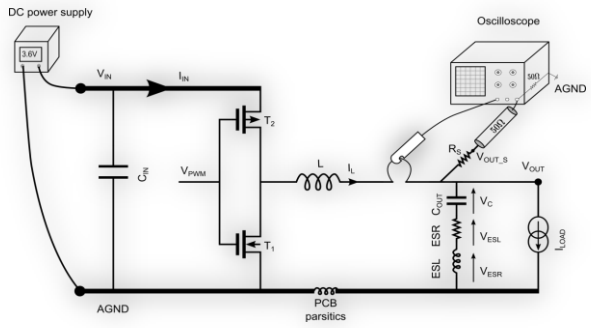
Most peripheries in portable electronics today tend to systematically employ high efficiency Switched Mode Power Supplies despite their inherent output noise. The power saving requirement today covers all front end IPs such as RF modems and RF transmitters and System Designers are required to tame SMPS switching noise and keep it under control from both points of view: frequency locus and noise magnitude.

PMIC designers usually delegate the specification of filtering components to Applications Engineers without necessarily providing sufficient theory elements to motivate the recommendations that are finally transcribed AS IS into the datasheet.

Electronic Engineers at the customer side could not only base their opinion on prior experience and empirical results. They would like to understand the reasons why such capacitor or inductor are used and what is the possible impact on their system performance, especially when it is a question of supplying sensitive devices such as an RF Modem or an RF Power Amplifier.

This short paper proposes an overview of the theory and techniques to be considered when selecting the filtering component of a DCDC converter especially the output capacitor. It also provides rules of thumb for selecting the right component and explains the relationship between its electrical characteristics and the DCDC output noise spectrum.

The paper is meant to be simple, although it includes some equations, and to provide simple and practical hints for Applications and System Engineers.



II. Sizing the filtering capacitor

In a DCDC converter such as a step down or buck converter operating in PWM mode (Figure 1), the sizing of the output capacitor depends on three parameters:

1) The voltage overshoot ΔVOS occurring at the end of the start-up phase especially when the inductor current hits the current limit before settling to permanent regime. (Figure 2)
2) The loop bandwidth which is dominated by the double poles formed by the LC filter
3) The voltage ripple induced by $\frac{\Delta I}{2}$, the amplitude of the inductor current ripple

The capacitance value is essentially determined by the output voltage overshoot because it results from the worst case condition of energy exchange between the inductor L and the capacitor C and it constitutes a worst case perturbation for the DCDC regulation loop. The capacitance value, once selected, will quite directly predicate the capacitance technology itself (MLCC, tantalum, or electrolytic) which consequently sets the value of the parasitic elements (ESL and ESR). With C, L, ESL, ESR, the designer should be able to

determine the shape of the output voltage ripple and describe the DCDC output noise spectrum as detailed hereafter.

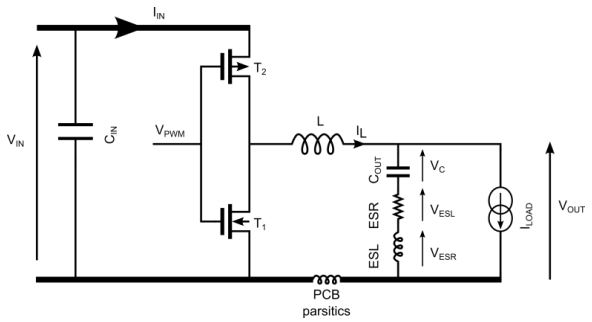


Figure 1. Output stage of a buck converter showing the parasitic elements of the output filter

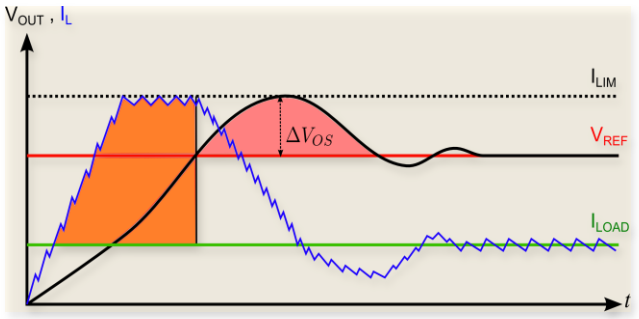


Figure 2. Voltage overshoot occurring at the end of the start-up phase in a DCDC converter.

We can give a fairly good estimation of the voltage overshoot magnitude occurring at the end of the start-up phase and thus determine the value of the capacitor required at the output. We assume that, during the start-up, the current in the inductor is limited to a maximum value I_{LIM} in order to prevent magnetic field saturation or prevent overheating. When the output voltage reaches a regulated value, the excessive energy stored in the inductor is entirely transferred to the output capacitor which results in a voltage overshoot as shown in Figure 2.

Equation (1) represents the energy exchange law between L and C_{OUT} in a worst case condition where no current is absorbed by the load.

$$\frac{1}{2}C_{OUT}\left(V_{OUT}+\Delta V_{OS}\right)^2=\frac{1}{2}C_{OUT}V_{OUT}^2+\frac{1}{2}LI_{LIM}^2 \qquad (1)$$

Where: C_{OUT} is the output capacitance, L is the inductance, V_{OUT} is the output voltage, I_{LIM} is the current limit and ΔV_{OS} is the overshoot in the output voltage of the converter.

In other terms, and assuming ΔV_{OS} is small compared to V_{OUT}, C_{OUT} can be written as follows

$$\frac{\Delta V_{OS}}{V_{OUT}}=\frac{1}{2}\frac{LI_{LIM}^2}{C_{OUT}V_{OUT}^2} \qquad (2)$$

Low voltage overshoot requires high C_{OUT}

The circuit designer can use equation (3) to select the value of C_{OUT} depending on the desired ΔV_{OS} and I_{LIM}.

Regarding the loop bandwidth (F_{LC}), C_{OUT} impacts the base position of the poles of the LC filter as follows:

$$F_{LC}=\frac{1}{2\pi\sqrt{L\times C_{OUT}}} \qquad (3)$$

Which will require a particular attention if larger bandwidth is needed.

A large DCDC loop bandwidth requires a low C_{OUT}

Notice that large bandwidth is often needed for fast response tracking.

At last, the DCDC output ripple represented by the peak to peak value ΔV_{OUT_PP} can be written as follows:

$$\Delta V_{OUT\_PP}=\frac{\Delta I.T_0}{8\times C_{OUT}}=V_{OUT}\frac{\pi^2(1-D)}{2}\left(\frac{F_{LC}}{F_0}\right)^2 \qquad (4)$$

Where: ΔI is the inductor's current ripple, D is the duty cycle, F_0 is the switching frequency and T_0 is the switching period. (C_{OUT} is assumed to be ideal)

A low output voltage ripple requires a large C_{OUT}

III. Close Analysis of the ripple voltage:

The output capacitor has in reality parasitic elements (ESL and ESR) that contribute in producing the ripple voltage. They alter both ripple amplitude and shape.

The corresponding waveforms shown in Figure 3 highlight the effect of each component on the overall ripple.

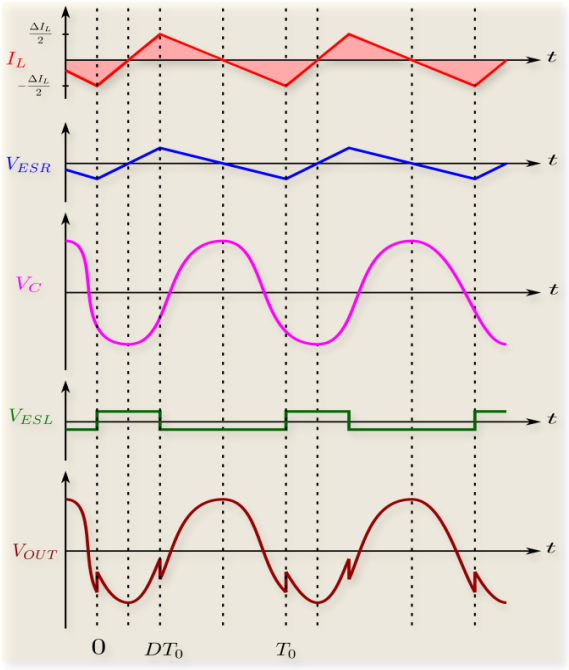


Figure 3. Detailed contributions of the parasitic elements to the output voltage ripple in a DCDC converter.

The assumption in this illustration is that the ESR effect has a smaller order of magnitude than the voltage produced by the capacitor itself, while the ESL induced voltage has much more effect on the capacitor voltage; this fairly applies to MLCC capacitors used in high frequency DCDCs today. More interestingly, it is shown that the ESL induced ripple results in changing the magnitude of the output ripple while it introduces sharp voltage variations and increases the high frequency and undesirable spectrum contents.

The total amplitude of the output ripple is given by:

$$\Delta V_{OUT\_PP} = \frac{\Delta I \times T_0}{8 \times C} + \frac{ESR^2 \times C \times \Delta I}{2T_0 D(1-D)} - \frac{ESL \times \Delta I}{D(1-D)T_0} \qquad (5)$$

The ESL reduces the amplitude of the voltage ripple

IV. Spectrum of the output ripple

In the case of RF transmitters the ripple voltage of the DCDC converter interferes with the carrier frequency due to the nonlinear behavior of the RFPA. The interference is mostly linked to the 3rd intermodulation effect IM3. However one has to consider the direct mixing effect ($F_{Carrier} \pm F_0$), ($F_{Carrier} \pm 2F_0$), ($2F_{Carrier} \pm F_0$) which could not be neglected due to the large "distance" between the carrier frequency (F_{TX}) and the switching frequency of the DCDC (F_0).

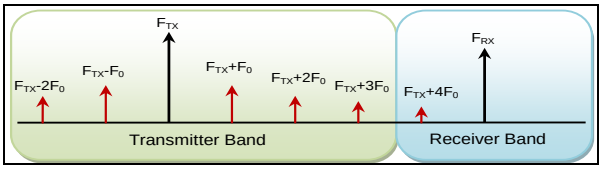


Figure 4. Transfer of the DCDC Noise to the RFPA band.

As a constraint, the designer has to prevent any interference with the adjacent channels where an RFPA has to show a rejection of 33dBc (first channel) [1] such as for 3G and 4G standards.

The designer would need to employ our theory to model the DCDC behavior and provide a better estimation of the ACLR (Adjacent Channel Leakage Ratio).

[1] 3rd Generation Partnership Project, "Evolved Universal Terrestrial Radio Access (E-UTRA), user Equipment (UE) radio transmission and reception," *3rd Generation Partnership Project*, TS 36.101 V11.1.0, 2012, [online]. Available: http://www.3gpp.org/ftp/Specs/archive/36_series/36.101/36101-b10.zip [accessed: 11,2013]

The full spectrum of the voltage ripple can be written using Fourier transform as follows:

$$V_{OUT}(nF_0) = \frac{\Delta I \,\mathrm{sinc}(\pi n D)}{1-D} \times \sqrt{\left(\frac{ESR}{\pi n}\right)^2 + \left(\frac{T_0}{2\pi^2 n^2 C} - \frac{2 \times ESL}{T_0}\right)^2} \quad (6)$$

Where: $V_{ESR}(nF_0)$, $V_{ESL}(nF_0)$, $V_C(nF_0)$ are the discrete Fourier transforms of the ESR, the ESL, and the Capacitor voltages respectively.

Figure 5 shows an example of detailed spectrum components calculated for a buck converter operating at 1 MHz and employing optimum L and C values:

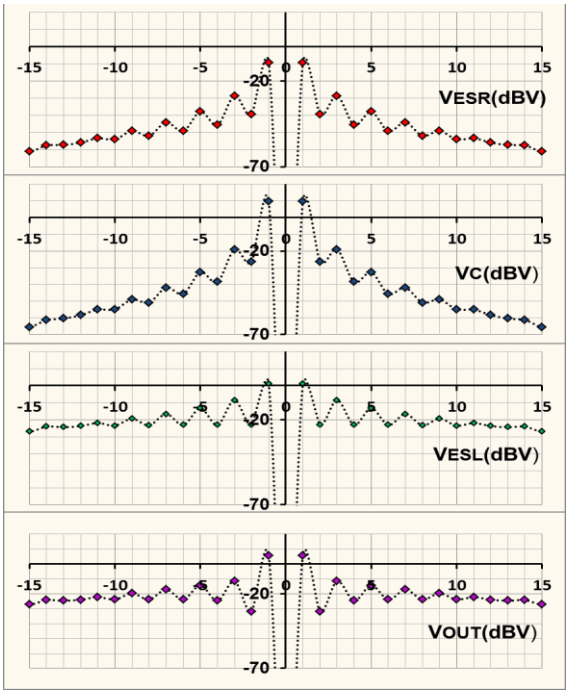


Figure 5. Detailed spectrum contents of the output voltage (V_{OUT}) with the contributions of each element of the capacitor model (V_C, V_{ESL}, V_{ESR}). The X axis represents the frequency in MHz.

Figure 5 reveals important spur amplitude across the ESL at the fundamental harmonic which is not translated into the same spur that effectively appears at the output voltage (bottom curve)!

To the same extents, the contribution of the ESL at higher harmonics reveals to be the dominating effect while none of the ESR or the C ripple components is relevant at this point!

The ESL related ripple dominates the High Frequency spurious contribution of the Output Voltage noise spectrum

V. Extracting the capacitor elements (C, ESR, and ESL)

Application engineers might have no time to measure the ESL, ESR or C_{OUT} knowing they are always different from the typical specifications stated in the manufacturer datasheet.

Nevertheless, this section gives simple techniques allowing quick and accurate extraction of the ESL, ESR and C_{OUT} directly by using an oscilloscope.

There are quick methods to estimate ESR, ESL and C_{OUT} by using oscilloscope measurements

Measurement Fixture

The main difficulty of measuring signals in DCDC converter is the noise caused by the switching of the power train in the presence of parasitic elements. The noise perturbs all the signals like the output voltage, the inductor current and the switching node voltage.

The noise can be even higher when we consider the perturbation brought to the input voltage of the DCDC and inherently fed back to the controller circuits. For this reason a big capacitor should be connected between the input voltage V_{IN} and the power ground PGND in order to filter that noise. (Typical value of C_{IN} is 10µF for 6MHz DCDCs or 22µF for 3MHz ones).

We propose to measure the capacitor and its parasitic elements by observing the output voltage and the inductor's current including their ripples.

Any measurement must be performed using a 50Ω matched connectors to the scope.

The use of high impedance probes is prohibited here because it attenuates the signal (already low) by 20dB.

High impedance probes have around 14pF and several nH parasitic which results in a resonance in the measured output voltage.

A 50 Ω series resistance is required to match the cable on the source side and prevent stationary waves.

Figure 6 shows the setup of the experiment with the details of the connections.

In our experiment, we took as an example a buck converter with the following parameters:

V_{IN}	V_{OUT} (V)	F_0 (MHz)	I_{LOAD} (mA)
3.6	1.8	2.4	300

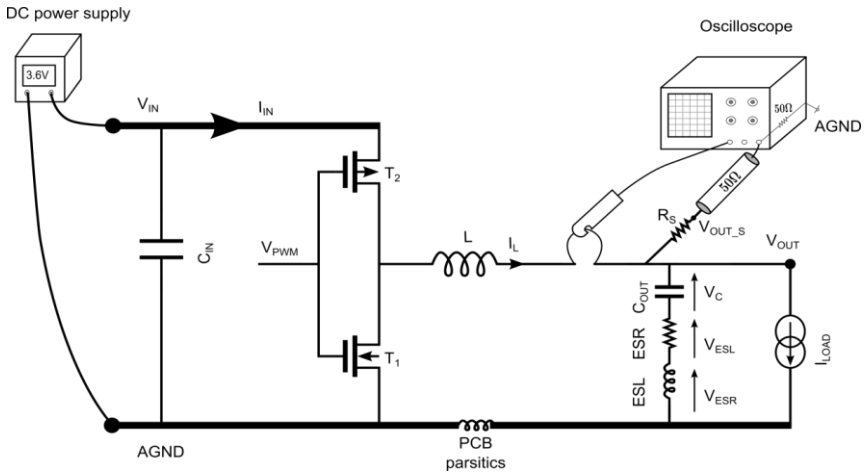


Figure 6. Measurement setup representing the output stage of a buck converter with the parasitic elements of the filtering capacitor and the scope setup allowing accurate measurement of the output voltage ripple. The 50Ω cable must be properly grounded to the PCB ground plane. Use R_S = 50 Ω for a probe attenuation factor of 6dB [2].

Measuring the Output Capacitor

A simple way to measure the output capacitor of a DCDC converter is to charge it completely to a certain voltage then discharge it in a known resistor connected in parallel to it and finally deriving the capacitance from the discharge time constant. The capacitor can be charged or discharged by turning the converter ON or OFF for some time.

In practice we can apply a square wave to the enable signal of the DCDC to switch it ON and OFF, then we take one cycle and we measure the slope of the discharging curve of the output voltage V_{OUT} by using the dV/dt function in the mathematics of the oscilloscope.

The equation of the capacitance is:

$$C_{OUT} = \frac{V_{OUT}}{R_P \times \frac{dV}{dt}}$$

Figure 7. Discharge cycle of the output capacitor

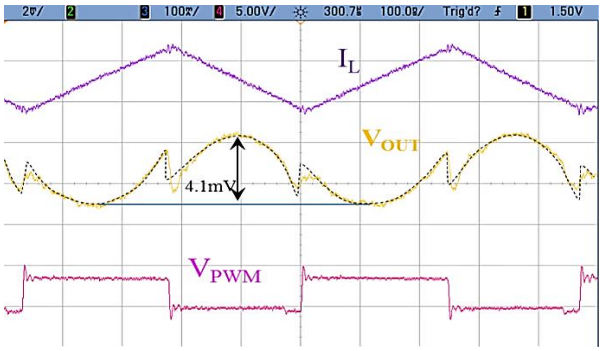


Figure 8. Experimental results for the buck converter. Dashed line is the expected waveform of the output voltage.

From the above figure $\frac{dV}{dt} = 85\ KV/sec$

R_P= 10 Ω, V_{OUT} = 1.8V

So C = 2.1µF

Measuring of the inductance:

Measuring the inductance value requires measuring the inductor's current and the output voltage. The current can be measured using a current probe, and the voltage can be measured as mentioned previously without missing the details of the ripple.

Using the oscilloscope we measure the values of V_{IN}, V_{OUT}, D, T_0, and ΔI:

In our example:

$V_{OUT\ S}$ (V)	ΔI (mA)	T0 (nsec)	D
1.5	135	410	0.54

$$V_{OUT} = \frac{6}{5} \times 1.5 = 1.8V$$

$$L = \frac{(V_{IN} - V_{OUT}) \times D \times T_0}{\Delta I}$$

$$L = \frac{(3.6 - 1.8) \times 220 \times 10^{-9}}{0.135} = 2.93\mu H$$

Note: Expect a series shunt in your PCB to be cut and replaced by a current measurement loop.

Measuring ESL

ESL can be extracted easily by measuring the sharp voltage step in the ripple voltage of few mV of V_{OUT}.

The equation of ESL is given by:

$$ESL = \frac{V_{STEP} \times D(1-D) \times T_0}{\Delta I}$$

Where,

V_{STEP} is the sharp voltage step in the output ripple.
V_{STEP} = 1.52*6/5 = 1.82 mV

ESL = 1.4nH

Measuring the ESR

After extracting the values of C_{OUT} and ESL we can use equation (6) to extract the value of ESR.

In our example: ESR= 5.7mΩ

VI. Conclusion

A simplified approach can be used by Design and Application Engineers to select the filtering capacitor for a DCDC converter. A simplified theory can also be used to understand the noise spectrum components of the DCDC output voltage. An illustration of the ESL effect in reducing the ripple voltage and generating high frequency harmonics is provided. Finally a simple and practical approach is provided to help application engineers perform fairly accurate measurements of the voltage ripple and exploit them to debug the DCDC performance.

External Links and References

[1] A. Fares, et al. “Simplified Review of DCDC Switching Noise and Spectrum Contents,” IEEE, PRIME 2014

[2] Aldrick S. Limjoc, “Measuring Output Ripple and Switching Transients in Switching Regulators” Application Note, http://www.analog.com/static/imported-files/application_notes/AN-1144.pdf

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